

SELECTIVE STATE RECONSTRUCTION

Seed State OS

Small state.
Focused reconstruction.

Reuse qualified retained structure.
Reconstruct the required changes.
Check before publishing results.

UK patent application GB2624953.2 (pending)

Recorded results and a proposed commercial route



THE PRODUCT OPPORTUNITY

Repeated state work creates an opportunity

When much of a structured state remains applicable, a system can focus on the changes and dependencies it needs.

Application state

Avoid repeating applicable preparation in a defined runtime.

Graphics and digital twins

Explore focused updates when scene state changes.

Embedded devices

Evaluate repeated state work on the intended controller or device.

Archives and recovery

Restore exact retained records, then qualify them for current use.

These are integration opportunities with workload-specific acceptance.

WHAT THE PRODUCT DOES

The state reconstruction workflow

A retained record becomes useful working state through an agreed reconstruction and verification path.

01 Identify useful state

Agree the state boundaries, dependencies and output contract.

03 Check before release

Verify required outputs and current applicability.

02 Reconstruct selected state

Reuse applicable structure and retain exact changes.

04 Continue the application

Supply the qualified state to the compatible consumer.

SAME-FPGA BOUNDED TASK

99.48% fewer FPGA engine cycles

Conventional scalar firmware versus native dataflow on the same bounded task and the same FPGA.

Native dataflow

13

2,523 → 13

median engine cycles

Scalar firmware

2,523

256 requests across both arms.
Zero incorrect complete outputs.

Complete service: 2.9465 → 2.331896 ms (1.264×). Input preparation was outside this comparison.

SELECTIVE GPU UPDATE

One changed tile among 4,096

A deterministic structured workload used the same GPU and the same operator across 32 rounds.

Logical work	Full dispatch	Selected update
Dispatched threads	536,870,912	131,072
Work-accounting traffic	12 GiB	3 MiB

4,096× less dispatched logical work

4,095 tiles remained applicable. Primary GPU execution ratios were 353–354× on the tested output arms.

Logical traffic differs from physical bus traffic. Operational update times are measured separately.

PRIMARY STUDY AND SEPARATE REPEAT

The operational GPU comparison

Mean paired operational-time ratios. Thirty paired trials per output arm in each study.

Output contract	Primary	Separate repeat
Full output materialised	22.4062×	20.9190×
Compact output	27.3896×	24.6871×

120/120 trial results matched exactly

Twenty hostile controls were refused with exact fallback. Zero false accepts.

Warm retained state. Initial construction and a 93–94 ms independent full-output evaluator were outside the timer.

RETAINED COMPATIBLE STATE

A compact CPU validation route

2,668×

shorter CPU validation time in a retained repeat study

96 compatible structured-state fixtures.
An existing local atlas and receipts remained available.

Each workload and timer remains separate from the FPGA and GPU results.

A separate measurement boundary

The original study recorded approximately 2,548×

This is route validation with retained dependencies. It is separate from initial construction and complete application execution.

SEPARATE REUSE STUDIES

Retaining useful structure adds value

Each result has its own workload and comparator. These percentages are not compounded.

Comparison	Recorded reduction
16-slot collection versus one slot	62.83% fewer collection cycles
Resident state versus optimised 16-slot cache	17.01% fewer resident-active cycles
Retained-transform reuse on recurring requests	31.51% fewer producer cycles
Complete mixed request corpus	20.42% fewer producer cycles

The optimised cache included hardware multiplication and equivalent current assertions.

Exact persistence can support returning state

One synthetic versioned-data workload compared the accepted archive/state component with two alternatives.

Implementation	Pipeline	Logical data	Allocated space
Archive/state component	135.98 s	32.51 MB	246.02 MB
Trained Zstandard	82.81 s	76.09 MB	289.41 MB
Borg + compaction	918.48 s	52.31 MB	445.78 MB

9,216 fresh reconstruction checks passed

57.3% fewer logical bytes than trained Zstandard. 37.9% fewer than compacted Borg.

Zstandard was faster on this workload. Installation and shared laboratory costs are additional.

PROSPECTIVE CUSTOMER APPLICATIONS

Several entry points for integration

Begin inside a system where repeated state work already matters.

AI and automation

Structured tool state and task dependencies, with application-owned meaning and access.

Digital twins and graphics

Affected state and compatible image-region updates.

Embedded and mobile

Repeated device operations, measured on the intended hardware.

Archives and recovery

Exact retained records and qualified reconstruction of returning state.

Each application needs its own complete-work quality, timing and resource comparison.

PROPOSED COMMERCIAL MODEL

Licensing the deployed capability

UK patent application GB2624953.2 is pending. BBF proposes non-exclusive integration licences.

Application and service teams

Annual runtime licence with defined deployments, capacity and support.

Device and platform makers

Development agreement, then per-shipped-device royalties or volume bands.

Combined BBF stack

An agreed bundle or a single eligible-savings ledger where appropriate.

Company ownership

BBF retains its technology. Customers receive the agreed usage or distribution rights.

Prices and OEM terms remain to be agreed. Technical ratios do not determine a customer invoice.

INVESTOR AND PARTNER DISCUSSION

The next integration milestones

Qualify one valuable state operation.

Priorities for a deployment programme:

- 01 Complete protected target-host integration and recovery.
- 02 Measure complete equivalent work against the best feasible baseline.
- 03 Agree deployment, support and a commercial licence.

Discuss your workload: www.beyondbruteforce.com | hello@beyondbruteforce.com